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EXAMINER
CAMPOS, YAIMA

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

	Application No.	Applicant(s)
Office Action Summary	10/656,639	DURRANT, PAUL
	Examiner	Art Unit	
	Yaima Campos	2185	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>20 February 2007</u>.

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-5,10-12,14,16,17,20,22,24-27,29 and 31-39* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-5,10-12,14,16,17,20,22,24-27,29 and 31-39* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☒ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All   b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

RESPONSE TO AMENDMENT

1.   The examiner acknowledges the applicant's submission of the amendment dated February 20, 2007. At this point claims 11-12, 22 and 26-27 have been amended, claims 6-9, 13, 15, 18-19, 21, 23, 28 and 30 have been cancelled and claims 31-39 have been added. There are 27 claims pending in the application; there are 3 independent claims and 24 dependent claims, all of which are ready for examination by the examiner.

OBJECTIONS TO THE SPECIFICATION

Claim Objections

2.   **Claim 31 and 33-34** are objected to because of the following informalities:

3.   As per **claim 31**, the word "location" (line 8) should be changed to read – locations-.

4.   .   As per **claims 33 and 34**, these claims are objected to as being of improper dependent form because claims 33 and 34 have been written to depend on themselves. Applicant is required to place the claims in proper dependent form and indicate on what specific claim; claims 33 and 34 are intended to depend.

5.   Appropriate correction is required.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

6.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. **Claims 31 and 33-37** are rejected under 35 U.S.C. 102(b) as being anticipated by Tetrick (US 6,003,112).

8. As per **claim 31**, Tetrick discloses A computer system including:

a processor; **["processor 101" (Figure 1 and related text)]**

a controller; **["bridge/memory controller 111" including "memory interface 150" (Figure 1 and related text)]**

a data communications facility interconnecting said processor and controller; and **["the processor 101 is coupled to a CPU bus 110 which transmits signals between processor 101 and other components in the computer system 100" (Col. 2, lines 35-38) "A bridge memory controller 111 is coupled to the CPU bus 110 and the memory 113" (Col. 2, lines 51-52) (Figure 1 and related text)]**

a volatile storage device having a plurality of locations for volatile storage of data, **["memory 113" (Figure 1 and related text) wherein "memory 113 may be a dynamic random access memory (DRAM), a static random access memory (SRAM) device, or other memory device" (Page 2, lines 39-39-41)]**

said controller being responsive to a command received from the processor to copy data from a first of said plurality of memory locations to a second of said plurality of memory location, **["the memory interface 150 operates to perform operation on the memory 113 that might otherwise be performed by execution of code in the processor 101, the memory interface 150 frees up CPU time in the processor 101 for executing application code" (Col. 2, lines 58-64) "according to a second embodiment of the**

present invention, the memory interface 150 operates to copy a data structure from a first location in the memory 113 to a second location in the memory 113 when a memory-to-memory copy is requested" (Col. 3, lines 3-7) wherein "the register file 420 includes a first address field 502 that stores a starting address of the block of memory containing the data structured. The register file 420 includes a length field 501 that stores the size of the block of memory that contains the data structure. The register files 420 also contains a second address field 503 that stores the destination address of where the data structure is to be copied" (Col. 6, lines 1-9)] responsive to memory access requests from said processor to determine a delay in access by said processor to one of said first and second memory locations, with said delay being dependent upon a type of said request and the location among said first and second memory locations to which said access is directed [With respect to this limitation, Tetrick discloses "Read cycles that occur to the destination address range before the memory operations have been completed have the address converted to t he corresponding address in the starting address range. Any write cycles that occur to the second location in memory before the memory operations have been completed are DEFERRED and are queued by the memory interface 150" (Col. 6, lines 41-47)].

9.   As per **claims 33 and 34** (New) The system as recited in claim 33 wherein the data is copied from said first memory location to said second memory location by using a peer-to-peer copy operation on the data communication facility; wherein said data communications facility supports direct memory access (DMA), and said peer-to-peer copy operation is performed by using a transaction analogous to DMA ["**according to a second embodiment of the present invention, the memory interface 150 operates to**

copy a data structure from a first location in the memory 113 to a second location in

the memory 113 when a memory-to-memory copy is requested" (Col. 3, lines 3-7)

wherein "the memory interface 150 operates to perform operation on the memory

113 that might otherwise be performed by execution of code in the processor 101,

the memory interface 150 frees up CPU time in the processor 101 for executing

application code" (Col. 2, lines 58-64)].

10.   As per **claim 35** (New), Tetrick discloses The system as recited in claim 31

wherein the controller maintains a record of copy operations that are currently in progress

[With respect to this limitation, Tetrick discloses "each of the resource units 410-413

has a corresponding register file 420-423. A resource allocating unit 430 is coupled

to each of the resource units 410-413... The resource allocating unit also includes an

index register 435 and completion queues 436" (Col. 5, lines 43-57) wherein "the

resource allocating unit 230 monitors the activities of each of the resource units 210-

213" (Col. 4, lines 4-18) and explains "the memory interface 150 may implement any

number of resource units where a plurality of operations may be performed on the

memory 113 simultaneously by the memory interface 150 when a plurality of

resource units are implemented" (Col. 5, lines 26-32)].

11.   As per **claim 36** (New), Tetrick discloses The system as recited in claim 31

wherein said request is a read request for said second memory location and the controller

redirects said read request to facilitate reading data from said first memory location

during processing of said command [Tetrick discloses "Read cycles that occur to the

destination address range before the memory operations have been completed have

the address converted to t he corresponding address in the starting address range"

(Col. 6, lines 41-47)].

12.   As per **claim 37**, Tetrick discloses The system of claim 31, wherein the first

controller delays a write request for the first random access memory location pending

completion of the command [**Tetrick discloses "any write cycles that occur to the**

addressed range before the memory operations have been completed are queued by

the memory interface 150. These operations could also result in a DEFERRED

cycle, where the memory interface 150 responds with completion status at a later

time" (Col. 5, lines 20-25)].

Claim Rejections - 35 USC § 103

13.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14.   **Claims 1-4, 10-12, 14, 16-17, 20, 22, 24-27, 29, and 38** are rejected under 35

U.S.C. 103(a) as being unpatentable by Tetrick (US 6,003,112) in view of Fujihira et al.

(5,278,965).

15.   As per **claims 1 and 22**, Tetrick discloses A computer system including:

a processor; [**"processor 101" (Figure 1 and related text)**].

a first controller; [**"bridge/memory controller 111" including "memory interface 150"**

(Figure 1 and related text)]

a random access memory having a plurality of locations for volatile storage of data; and

[**"memory 113" (Figure 1 and related text) wherein "memory 113 may be a dynamic**

**random access memory (DRAM), a static random access memory (SRAM) device,
or other memory device" (Page 2, lines 39-39-41)]**

a data communications facility interconnecting said processor, said first controller, and
said random access memory; **["the processor 101 is coupled to a CPU bus 110 which
transmits signals between processor 101 and other components in the computer
system 100" (Col. 2, lines 35-38) "A bridge memory controller 111 is coupled to the
CPU bus 110 and the memory 113" (Col. 2, lines 51-52) (Figure 1 and related text)]**
wherein said first controller is responsive to a command received from the processor to
commence transmission of a quantity of data from a first random access memory location
to a second random access memory location, wherein said command specifies said first
and second random access memory locations, **["the memory interface 150 operates to
perform operation on the memory 113 that might otherwise be performed by
execution of code in the processor 101, the memory interface 150 frees up CPU time
in the processor 101 for executing application code" (Col. 2, lines 58-64) "according
to a second embodiment of the present invention, the memory interface 150 operates
to copy a data structure from a first location in the memory 113 to a second location
in the memory 113 when a memory-to-memory copy is requested" (Col. 3, lines 3-7)]**

Tetrick does not disclose expressly with the first controller monitoring operation
of the processor to terminate the transmission of the data to the second random access
memory location, during transmission of the quantity thereto, in response to the processor
generating a write request to the second random memory location.

Fuhijira discloses "with the first controller monitoring operation of the processor
to terminate the transmission of the data to the second random access memory location,

during transmission of the quantity thereto, in response to the processor generating a

write request to the second random memory location" as **["during the DMA transfer**

between two memories, it is possible to make a normal interruption of the DMA

transfer as if the interrupt request signal DONE is generated, by making a write

operation with respect to the register 18 from the CPU 50" and explains "in this

state where the DMA transfer is made. the CPU 50 outputs the chip select signal CS

responsive to an external interrupt request. In a step S1, the CPU 50 discriminates

whether or not a write operation is made with respect to the register 18... when the

discrimination result in the step S1 becomes YES, the data handler 17 in a step S2

supplies the terminate request signal CLS to the request handler 15" (Col. 6, lines

13-21; Col. 5, lines 49-64; Figure 5 and related text)].

Tetrick (US 6,003,112) and Fujihira et al. (US 5,278,965) are analogous art

because they are from the same field of memory access and control.

At the time of the invention it would have been obvious to a person of ordinary

skill in the art to modify the internal memory transfer system which uses a controller to

perform memory transfer/copy operations as taught by Tetrick, and further cancel DMA

transmission of data when a write request has been generated as taught by Fujihira.

The motivation for doing so would have been because Fujihira also teaches

["according to the direct memory access controller of the present invention, it is

possible to make a normal termination during a direct memory access transfer

regardless of whether or not a memory involved in the direct memory access

transfer has a function of generating a normal termination request signal. Further

the normal termination request signal can be made at an arbitrary timing" (Col. 2,

lines 6-28)].

Therefore, it would have been obvious to combine Fujihira et al. (US 5,278,965)

with Tetrick (US 6,003,112) for the benefit of performing internal memory transfers to

obtain the invention as specified in claims 1 and 22.

16.   As per **claim 2**, the combination of Tetrick and Fujihira discloses The system of

claim 1, wherein said random access memory is coupled to said data communications

facility via a memory controller, said memory controller configured manage operations

for said random access memory [**Tetrick discloses "the memory interface 150 operates**

to perform operation on the memory 113 that might otherwise be performed by

execution of code in the processor 101, the memory interface 150 frees up CPU time

in the processor 101 for executing application code" (Col. 2, lines 58-64) **"according**

to a second embodiment of the present invention, the memory interface 150 operates

to copy a data structure from a first location in the memory 113 to a second location

in the memory 113 when a memory-to-memory copy is requested" (Col. 3, lines 3-

7)].

17.   As per **claims 3 and 24**, the combination of Tetrick and Fujihira discloses The

system of claim 2, wherein the data is copied from the first random access memory

location to the second random access memory location by an internal memory transfer,

without traveling over the data communications facility [**"the memory interface 150**

operates to copy a data structure from a first location in the memory to a second

location in the memory 113 when a memory-to-memory copy is requested" (Col. 3,

lines 4-7) and explains "the memory copy operation can copy the data structure at

the first location in memory to the second location in memory any known

techniques" (Col. 35-38)].

18.   As per **claim 4**, the combination of Tetrick and Fujihira discloses The system of

claim 2, wherein said first controller is provided by said memory controller [**Tetrick**

discloses "bridge/memory controller 111" including "memory interface 150" (Figure

1 and related text)].

19.   As per **claims 10 and 25**, the combination of Tetrick and Fujihira discloses The

system of claim 1, wherein the processor continues processing operations prior to data

being completely copied to the second random access memory location [**Tetrick**

discloses "the memory interface 150 operates to perform operation on the memory

113 that might otherwise be performed by execution of code in the processor 101,

the memory interface 150 frees up CPU time in the processor 101 for executing

application code" (Col. 2, lines 58-64).

20.   As per **claims 11 and 26**, the combination of Tetrick and Fujihira discloses The

system of claim 10, wherein the first controller redirects a read request for the second

random access memory location to the first random access memory location during

processing of said command [**Tetrick discloses "Read cycles that occur to the**

destination address range before the memory operations have been completed have

the address converted to t he corresponding address in the starting address range"

(Col. 6, lines 41-47)].

21.   As per **claims 12 and 27**, the combination of Tetrick and Fujihira discloses The

system of claim 10, wherein the first controller delays a write request for the first random

access memory location pending completion of the command [**Tetrick discloses "any**

write cycles that occur to the addressed range before the memory operations have been completed are queued by the memory interface 150. These operations could also result in a DEFERRED cycle, where the memory interface 150 responds with completion status at a later time" (Col. 5, lines 20-25)].

22.   As per **claims 14 and 29**, the combination of Tetrick and Fujihira discloses The system of claim 1, further comprising a cache, and wherein any cache entry for the second random access memory location is invalidated in response to said command **[Tetrick discloses "cache 102" and explains "the cache 102 speeds up memory accesses by the processor 101 by taking advantage of its locality of access" (Col. 2, lines 47-49) wherein "the resource units 210-213 operate to update the status of the cache in the processor 101 corresponding to locations memory defined by information in their register files 220-223. The status of the cache data is updated to reflect that the processor no longer has a current copy of the contents in its cache"** (Col. 4, lines 61-66; Col. 43, lines 43-67)].

23.   As per **claim 16**, the combination of Tetrick and Fujihira discloses The system of claim 14, wherein any updated cache entry for the first memory random access location is flushed to memory in response to said command **[With respect to this limitation, Tetrick discloses "Memory interface 150 operates to copy a data structure at a first location in the memory 113 to the second location in the memory 113" (Col. 5, lines 43-47) wherein "the resource units 410-413 operate to read the data structure in the first locations in memory 113 defined by information in their register files 420-423... If write-back data is returned in response to the READ FOR OWNERSHIP cycle, the data is treated just as normal write-back. The bridge memory controller**

converts the read operation into a memory write and alters memory 113" (Col. 6,
lines 20-37)].

24.   As per **claim 17**, the combination of Tetrick and Fujihira discloses The system of
claim 1, wherein said processor supports a specific programming command to copy data
from a first random access memory location to a second random access memory location
["**the memory interface 150 operates to copy a data structure from a first location in
the memory to a second location in the memory 113 when a memory-to-memory
copy is requested**" (Col. 3, lines 4-7)].

25.   As per **claims 20**, the combination of Tetrick and Fujihira discloses The system of
claim 1, wherein said first controller transmits an acknowledgement of said command
back to the processor, and wherein the processor is responsive to a failure to receive said
acknowledgement within a predetermined time-out period to perform said copy operation
by issuing separate read and write commands.

26.   As per **claim 38** (New), Tetrick discloses The system as recited in claim 31 but
does not disclose expressly wherein transmission of a quantity of data from a said first
memory location to said second memory location occurs in response to said command
and said request is a write request directed to said second memory location with said
controller being responsive to said write request to terminate said transmission of said
data to the second random access memory location, during transmission of the quantity
thereto, in response to said write request.

Fuhijira discloses "with the first controller monitoring operation of the processor
to terminate the transmission of the data to the second random access memory location,
during transmission of the quantity thereto, in response to the processor generating a

write request to the second random memory location" as **["during the DMA transfer
between two memories, it is possible to make a normal interruption of the DMA
transfer as if the interrupt request signal DONE is generated, by making a write
operation with respect to the register 18 from the CPU 50"** and explains **"in this
state where the DMA transfer is made. the CPU 50 outputs the chip select signal CS
responsive to an external interrupt request. In a step S1, the CPU 50 discriminates
whether or not a write operation is made with respect to the register 18... when the
discrimination result in the step S1 becomes YES, the data handler 17 in a step S2
supplies the terminate request signal CLS to the request handler 15"** (Col. 6, lines
13-21; Col. 5, lines 49-64; Figure 5 and related text)].

Tetrick (US 6,003,112) and Fujihira et al. (US 5,278,965) are analogous art
because they are from the same field of memory access and control.

At the time of the invention it would have been obvious to a person of ordinary
skill in the art to modify the internal memory transfer system which uses a controller to
perform memory transfer/copy operations as taught by Tetrick, and further cancel DMA
transmission of data when a write request has been generated as taught by Fujihira.

The motivation for doing so would have been because Fujihira also teaches
**["according to the direct memory access controller of the present invention, it is
possible to make a normal termination during a direct memory access transfer
regardless of whether or not a memory involved in the direct memory access
transfer has a function of generating a normal termination request signal. Further
the normal termination request signal can be made at an arbitrary timing"** (Col. 2,
lines 6-28)].

Therefore, it would have been obvious to combine Fujihira et al. (US 5,278,965) with Tetrick (US 6,003,112) for the benefit of performing internal memory transfers to obtain the invention as specified in claim 38.

27.   **Claims 5 and 32** are rejected under 35 U.S.C. 103(a) as being unpatentable over Tetrick (US 6,003,112) and Fujihira et al. (US 5,278,965) as applied to claim 1 above, and over Tetrick (US 6,003,112) as applied to claim 31 above, and further in view of Busser et al. (US 6,732,243).

28.   As per **claims 5 and 32**, the combination of Tetrick and Fujihira discloses "a computer system" as disclosed in claim 1 [**See rejection to claim 1 above**] and a computer system as disclosed in claim 31 [**See rejection to claim 31 above**], respectively, but does not disclose expressly that wherein a first portion of the random access memory is coupled to said data communications facility via a first memory controller and includes said first random access memory location, and a second portion of random access memory is coupled to said data communications facility via a second memory controller and includes said second random access memory location.

Busser discloses a system and method wherein "a first portion of memory is coupled to said data communications facility via a first memory controller and includes said first memory location, and a second portion of memory is coupled to said data communications facility via a second memory controller and includes said second memory location". Busser teaches a [**method and apparatus for mirroring data in a storage system (Column 4, lines 44-45)**] including [**"a first controller management module" (Column 4, lines 45-46) and "a second controller management module" (Column 4, lines 51-52) wherein the "first controller memory module" has "a first**

memory" (Column 13, lines 63-67) and the "second controller memory module" has
"a second memory" (Column 14, lines 1-3)]. Busser also teaches that ["data is
mirrored from the first controller management module to the second controller
management module" (Column 4, lines 48-61)] and that [the controllers are
connected to a bus (Column 2, line 12)].

Tetrick (US 6,003,112), Fujihira et al. (US 5,278,965) and Busser et al. (US
6,732,243) are analogous art because they are from the same field of endeavor of
copying/transferring data from one memory location to another.

At the time of the invention it would have been obvious to a person of ordinary
skill in the art to make the system for transferring data from one memory location to
another as taught by Tetrick, cancel DMA transmission of data when a write request has
been generated as taught by Fujihira and further include two different controllers, one
controlling a first memory location and the other controlling a second memory location,
as described by Busser.

The motivation for doing so, as taught by Busser, would have been that by having
two different "controller management modules" controlling each of two different
memory locations, ["data is mirrored from the first controller management module
to the second controller management module using the first direct memory access
engine while avoiding interruption to the second processor" (Column 4, lines 58-61)
and vice versa]. Busser also teaches that this approach is useful because it ["reduces the
processing overhead involved with mirroring data" (Column 4, lines 38-39)].

Therefore, it would have been obvious to combine Busser et al. (US 6,732,243)
with Tetrick (US 6,003,112) and Fujihira et al. (US 5,278,965) for the benefit of creating

a system and method for transferring data from one memory location to another to obtain

the invention as specified in claims 5 and 32.

29.   **Claims 20 and 39** are rejected under 35 U.S.C. 103(a) as being unpatentable over

Tetrick (US 6,003,112) and Fujihira et al. (US 5,278,965) as applied to claim 1 above,

and over Tetrick (US 6,003,112) as applied to claim 31 above, and further in view of

Garret et al. (6,408,369).

30.   As per **claims 20 and 39**, the combination of Tetrick and Fujihira discloses "a

computer system" **[See rejection to claim 1]** and Tetrick discloses the computer system

of claim 31 **[See rejection to claim 31]** but does not disclose expressly "wherein said

first controller transmits an acknowledgement of said single command back to the

processor, and wherein the processor is responsive to a failure to receive said

acknowledgement within a predetermined time-out period to perform said copy operation

by issuing separate read and write commands."

Garret discloses "wherein said first controller transmits an acknowledgement of

said single command back to the processor, and wherein the processor is responsive to a

failure to receive said acknowledgement within a predetermined time-out period to

perform said copy operation by issuing separate read and write commands" as **["the**

controller returns a _command not completed_ back to the host computer and the host

computer can either try the operation again, or transfer the data using a _prior art_

command sequence" (Columns 3-4, lines 66-67 and 1-3) where the _"prior art_

command sequence" involves "reading data from one disk drive unit into its own

memory and then writing the data from its own memory to a second disk drive

unit" (Column 1, lines 14-16)].

Tetrick (US 6,003,112), Fujihira et al. (US 5,278,965) and Garret et al.

(6,408,369) are analogous art because they are from the same field of endeavor of

copying/transferring data from one memory location to another.

At the time of the invention it would have been obvious to a person of ordinary

skill in the art to make the system for transferring data from one memory location to

another as taught by Tetrick, cancel DMA transmission of data when a write request has

been generated as taught by Fujihira and further "wherein said first controller transmits

an acknowledgement of said single command back to the processor, and wherein the

processor is responsive to a failure to receive said acknowledgement within a

predetermined time-out period to perform said copy operation by issuing separate read

and write commands" as taught by Garret.

The motivation for doing so is because Garret discloses ["**the controller returns**

a *command not completed* **back to the host computer and the host computer can**

either try the operation again, or transfer the data using a *prior art* **command**

sequence" (Columns 3-4, lines 66-67 and 1-3) where the *"prior art* **command**

sequence" involves "reading data from one disk drive unit into its own memory and

then writing the data from its own memory to a second disk drive unit" (Column 1,

lines 14-16) to thereby save CPU processing time and accurately track completion of

memory transfers].

Therefore, it would have been obvious to combine Garret et al. (US 6,408,369)

with Tetrick (US 6,003,112) and Fujihira et al. (US 5,278,965) for the benefit of creating

a system and method for transferring data from one memory location to another to obtain

the invention as specified in claims 20 and 39.

ACKNOWLEDGMENT OF ISSUES RAISED BY THE APPLICANT

Response to Amendment

31.   Applicant's arguments filed February 20, 2007 with respect to the combination of

Garret and McKenny being improper have been fully considered and are persuasive.

Therefore, the rejection has been withdrawn. However, upon further consideration, a new

ground(s) of rejection is made.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

32.   The following is a summary of the treatment and status of all claims in the

application as recommended by **M.P.E.P. § 707.07(i)**

a(1) CLAIMS REJECTED IN THE APPLICATION

33.   Per the instant office action, **claims 1-5, 10-12, 14, 16-17, 20, 22, 24-27, 29 and**

31-39 have received a second action on the merits and are subject of a final rejection.

34.   For at least the above reasons it is the examiner's position that the applicant's

claims are not in condition for allowance.

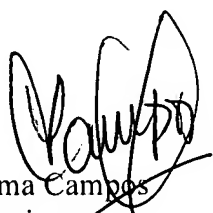## DIRECTION OF ALL FUTURE REMARKS

35.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Yaima Campos whose telephone number is (571) 272-

1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

IMPORTANT NOTE

36.   If attempts to reach the above noted Examiner by telephone are unsuccessful, the

Examiner's supervisor, Mr. Sanjiv Shah, can be reached at the following telephone

number: Area Code (571) 272-4098.

37.   The fax phone number for the organization where this application or proceeding is

assigned is 571-273-8300. Information regarding the status of an application may be

obtained from the Patent Application Information Retrieval (PAIR) system. Status

information for published applications may be obtained from either Private PAIR or

Public PAIR. Status information for unpublished applications is available through

Private PAIR only. For more information about the PAIR system, see http://pair-

direct.uspto.gov. Should you have questions on access to the Private PAIR system,

contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

April 26, 2007

Yaima Campos
Examiner
Art Unit 2185

SANJIV SHAH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100